IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Ivan Duzevik et al.

Application No.: 10/755,011 | Confirmation No.: 7721

Filed: January 8, 2004 | Art Unit: 2816

For: TERMINATION SENSE-AND-MATCH DIFFERENTIAL DRIVER | Examiner: K. B. Wells

DECLARATION OF IVAN DUZEVIK UNDER 37 C.F.R. § 1.132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Ivan Duzevik, declare as follows:

1. I am a Circuit Design Engineer for National Semiconductor Corporation.

2. I have been employed with National Semiconductor Corporation since June of 2001.

3. I have a B.S. in Electrical Engineering from the University of Southern Maine.

4. I have over 5 years of experience in the field of analog circuit design. I have a high degree of familiarity with low-voltage differential signaling (LVDS) interfaces.

5. I am one of the inventors for the above-referenced application.

6. National Semiconductor Corporation is the assignee for all of my rights in the above-referenced application.

7. I have reviewed U.S. Patent 6,380,797 (hereinafter referred to as Macaluso I), U.S. Patent 6,600,346 (hereinafter referred to as Macaluso II), U.S. Patent 6,356,141 (hereinafter referred to as Yamauchi).

In my expert opinion, based on my thorough review of the Yamauchi reference, the following statements (8-10) are true:

8. Gate voltage control circuit 30 of Fig. 1 of Yamauchi does not affect the source resistance of the output driver circuit (as seen from the output terminals). Rather, in the circuit of Fig. 1 of Yamauchi, gate voltage control circuit 30 makes adjustments to the current drive capability of driver 10 by controlling the gate voltages Vgp and Vgn in such a way that the variation due to a change in bias voltage Vm is compensated. The source resistance seen from the output terminals is not affected by the changes to gate voltages Vgp and Vgn.

9. Transistor 11 of Fig. 1 of Yamauchi operates in the saturation region of operation. The circuit of Fig. 1 would not function properly if transistor 11 of Yamauchi were biased in the linear region of operation. Although transistor 11 may operate in the linear region of operation for very brief period of time, the feedback provided by gate voltage control circuit 30 almost immediately changes the operation back to the saturation region of operation when such a condition occurs. An example of this is described in Column 5, lines 14-33 of Yamauchi. As described in this section, the operation point may move from a saturation region of operation to a linear region of operation, at which point, the gate voltages are adjusted to move the operation point back into a saturation region of operation, so that the circuit will function properly.

10. Transistor 14 of Fig. 1 of Yamauchi operates in the saturation region of operation. The circuit of Fig. 1 would not function properly of transistor 14 of Yamauchi were biased in the linear region of operation. Although transistor 14 may operate in the linear region of operation for very brief period of time, the feedback provided by gate voltage control circuit 30 almost immediately changes the operation back to the saturation region of operation when such a condition occurs.

In my expert opinion, based on my thorough review of the Macaluso I reference, the following statements (11-12) are true:

11. In FIG. 2 of Macaluso I, the source resistance as seen by the output terminals does not track the termination resistance. The output driver transistors M88, M89, M90, and M91 operate to provide an output source resistance (as seen by the output terminals) independent of the line termination.

12. Transistors M94, M84, and M92 of FIG. 2 of Macaluso I each operate in the saturation region of operation. In FIG. 2 of Macaluso I, transistors M94, M92, M84 provide constant current (tail current sources and sinks) for the transistors in the driver (102) and the replica circuit (103) respectively. If the transistor M94 falls out of saturation, the control circuit (103) will correct the gate voltage of the transistor and bring M94 back to saturation. If the transistors M84 and M92 fall out of saturation, the control circuit (104) will correct the gate voltage of M84 and M92 and bring M84 and M92 back to saturation. For correct switching, the driver transistors (M88-M91) should be supplied by a constant current. The tail current sources (M94, M84, and M92) provide constant current when they operate in the saturation region. Consequently, the each of the driver transistors (M88-M91) has a drain-to-source resistance that is independent of the output termination.

In my expert opinion, based on my thorough review of the Macaluso II reference, the following statements (13-14) are true:

13. In FIG. 2 of Macaluso II, the source resistance as seen by the output terminals does not track the termination resistance. The output driver transistors M0, M1, M2, and M3 operate to provide an output source resistance (as seen by the output terminals) independent of the line termination.

14. Transistors M9, M10, M6, and M8 of FIG. 2 of Macaluso II each operate in the saturation region of operation. In FIG. 2 of Macaluso II, transistors M9, M10, M6, and M8 provide constant current (tail current sources and sinks) for the transistors in the driver circuitry (12a) and the replica biasing circuitry (14a) respectively. If the transistor M9, M10, M6, and/or M10 falls out of saturation, the replica biasing circuitry (14a) will correct the gate voltage of the transistor and bring the transistor back to saturation. For correct switching, the driver transistors (M0-M3) should be supplied by a constant current. The tail current sources (M9 and M10) provide constant current when they operate in the saturation region. Consequently, the each of the driver transistors (M0-M3) has a drain-to-source resistance that is independent of the output termination.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these

statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Dated: November 8, 2005

By /Ivan Duzevik/
Ivan Duzevik

/Ivan Duzevik/

/Terri L Mingo/

TERRI L. MINGO
NOTARY PUBLIC, MAINE
MY COMMISSION EXPIRES
NOVEMBER 9, 2008